Mathematical Model Development for Faults Simulation in Current-source PWM Inverters

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***Abstract*—Despite of remarkable technological achievements reached in power electronics (both for devices and circuits) faults remains inevitable, being the main cause of power systems interrupts and failures. In the last decade the fault problem in power electronics has been investigated with more attention both from theoretical and experimental point of view. Following these trends, this paper is focused to introduce a novel mathematical model specially developed for simulation of faults in current-source inverters (CSIs) operating in high reliability servo-drive applications. By approaching a generalized fault-tolerant model development, it has been designed a CSI model able to simulate both unfaulty and faulty conditions when one or more power electronic devices fails in operation. In this way the drawback of building a separately model and a separately simulation program for each operation mode (both for unfaulty and faulty states) has been eliminated. The generalized model has been validated via careful computer-aided simulations in Matlab/Simulink software environment. In order to compare the obtained results in different failure states various faulty-state power converter architectures has been considered, their operating conditions being tested in a servo-drive application.**

Keywords*—*mathematical model; fault-tolerant; current-source inverter; device failure; self-reconfiguration.

I. INTRODUCTION

It is well known that increasing safety and performance requirements in modern servo-drive applications lead to more and more complex control systems, which make faults inevitable. Moreover, in critical servo systems the reliability of the drive is very important where faults are impermissible, unwanted faults may cause loss of the human life or capital. As main parts of modern electrical drive systems, power electronic converters play a key role in the entire energy transferring process and driving application flow. It is no doubt the last decades achieved technological improvements in power electronics (as for new devices, as for new circuits, control systems and protection strategies) are remarkable but faults remain unavoidable in each case, being the main cause of power system interruptions, failures, or damages [1, 2].

However, fault detection and isolation, respectively the fault elimination in power electronic converters is not an easy task, so fault occurrence implies long time intervals in which the power converter must remain out of service. At the same time, fault diagnosis and fault elimination in such a complex electronic systems requires high level knowledge of the topic and adequate experimental skills, as well. The above requirements are particularly true for all that power electronic converters which also embeds complex integrated control circuits or microprocessor-based supervisor boards [3, 4]. Obviously, fault investigation and detection always implies the consideration of the effect of faults on power devices, on other active- and passive circuits in the converter, or on electric-electronic systems which are interconnected with the faulted power electronic module.

From other point of view, in international references still dominate the approach which considers each fault as a separate and isolated case without a general vision on the rest of the electronic system. This means that the great majority of studies regards on a single device investigation, where the diagnosis, localization, and reparation efforts are concentrated [5, 6, 3]. Obviously, such strategies denotes that in the topic of fault-tolerance investigation in power converter systems the researches are still in full evolution, without clearly established and generally accepted theories and methods by the engineering community involved. This observation remains even it is well known that a great amount of technical literature is already available in this research area. In spite of all these, it is no doubt that same important questions are still under careful consideration or many issues are waiting for answer from scientists involved in the topic.

II. FAULT-TOLERANCE PROBLEM STATEMENT IN POWER CONVERTERS

According to a general rule classification faults in power converter systems may be categorized as follows: a single power device (or switch) short circuit, a converter leg short circuit, one power device open circuit, or one converter leg open circuit. It is well known that short circuits in silicon devices implies the irreversible destruction of one or more components and open circuit faults causes the losses of control (switching pulses) against the power devices interested. Short circuits are very fast events (mostly in range of microseconds) and there is no time to interrupt and isolate them by using software solutions. Usually they are managed via direct hardware solutions by using additional fast switching devices, or ultra fast fuses without introducing additional inductance in the considered main circuits [7]. However, it is important to mention here that short circuit faults evolution converges always to an open circuit fault in a very short time. In other words, if their effects on transients can be considered neglected, they turns quickly into a permanent state open circuit fault. This is the reason for why in the vast majority of international references only the open circuit faults and their effects are considered [4, 5, 6].

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Furthermore, in the vast majority of cases at least two separately simulation models are used in power electronic systems: one for healthy (unfaulty) situation and another which considers the faulty state. This strategy implies the careful management of a two separate programs, where the state space variables of the unfaulted model are collected and used then as initial values for the second model at faulty condition. In fact, this operation means to stop the simulations made with the unfaulty model and to restart it then by using the second model at faulty conditions. Obviously, in most of cases this is a very inconvenient and time consuming task as well. Hence, to develop a generalized mathematical model suitable to merge the two different operation modes of power electronic converters looks a welcoming idea to overcome the above mentioned shortcomings or bottlenecks.

III. A GENERALIZED MATHEMATICAL MODEL FOR FAULTS SIMULATION IN PWM CURRENT-SOURCE INVERTERS

Starting from the theoretical remarks mentioned in the previous paragraph, let's consider in the first step of this study a classical H-bridge configuration of a power converter unit, were the load circuit is inductive (for example a motor winding) with the parameters *R* and *L*, as shown in Fig. 1.

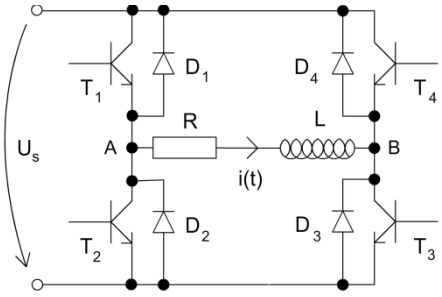

Figure 1. A classical H-bridge electronic configuration

It is well known that by consecutively pulse width modulation (PWM) switching commutation of the transistor couples T_1 and T_3, respectively T_2 and T_4, this bridge can operate as an asynchronous (bang-bang) current-source inverter, according to the current and voltage waveforms presented below in Fig. 2.

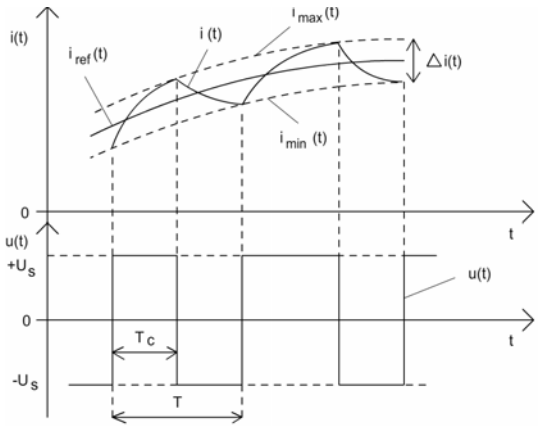

Figure 2. The well known operation principle of a bang-bang current-source PWM inverter

By measuring the load current and comparing it with a reference imposed ($i_{ref}(t)$ in figure 2),

$$u(t) = \begin{cases} +U_s \text{ if } i(t) \le i_{min} = i_{ref}(t) - \Delta i(t)/2 \\ -U_s \text{ if } i(t) \ge i_{max} = i_{ref}(t) + \Delta i(t)/2 \end{cases}, \quad (1)$$

where

$$\Delta i(t) = i_{max} - i_{min}, \quad \text{respectively} \quad (2)$$

$$i(t) = \begin{cases} \frac{U_s - E}{R} \cdot \left(1 - e^{-\frac{t}{\tau}}\right) + i_{min} \cdot e^{-\frac{t}{\tau}}, & 0 < t < T_c \\ -\frac{U_s + E}{R} \cdot \left(1 - e^{-\frac{t-T_c}{\tau}}\right) + i_{max} \cdot e^{-\frac{t-T_c}{\tau}}, & T_c < t < T \end{cases} \quad (3)$$

where $\tau = L/R$, and E is the induced electromagnetic voltage in the winding.

In international references usually the faulty conditions are modeled by considering power electronic systems as a set of active components with instantaneous commutation for which it is possible to define a "switching function" as follows [4, 5, 6, 7]:

$$Swf = \begin{cases} 1, & if \ \ a\ driving\ pulse\ is\ given \\ 0, & otherwise \end{cases}. \quad (4)$$

In case of the H-bridge configuration from Figure 1 the switching functions for the transistors (or active components) are:

$$Swf_{T_i} = \begin{cases} 1, & if \ \ a\ driving\ pulse\ is\ given \\ 0, & otherwise, \ for\ j = 1 \div 4 \end{cases}. \quad (5)$$

Towards, the conduction state of the free-wheeling diodes depends on the current sign (for example the diode D_1 conducts the negative current only the controllable device T_2 is turned off), therefore the switching function for the diode D_1 is:

$$Swf_{D_1} = \overline{Swf_{T_2}} \odot i_-, \text{ where} \quad (6)$$

i_- represents the negative instantaneous current (flows from point *B* to *A*), the notation "⊙ "meaning a logical *AND* operator, and the sign – over the T_2 transistor's switching function represents a logical *NOT* operator. In the same way are defined the switching functions for the rest of free-wheeling diodes, for example:

$$Swf_{D_2} = \overline{Swf_{T_1}} \odot i_+. \quad (7)$$

Summarizing the above introduced functions, results that for the four bidirectional switches (including the conducting transistor and diode) it is possible to write:

$$\begin{aligned} Swf_1 &= [Swf_{T_1} \odot i_+] \oplus [\overline{Swf_{T_2}} \odot i_-] \\ Swf_2 &= [Swf_{T_2} \odot i_-] \oplus [\overline{Swf_{T_1}} \odot i_+] \\ Swf_3 &= [Swf_{T_3} \odot i_+] \oplus [\overline{Swf_{T_4}} \odot i_-] \\ Swf_4 &= [Swf_{T_4} \odot i_-] \oplus [\overline{Swf_{T_3}} \odot i_+]. \end{aligned} \quad (8)$$

In equations (8) the term at the left of the operator *OR* (notated with "⊕") regards the controllable devices conduction of a positive or negative current, while the right the diode conduction. This is self-evident by considering that an equivalent bidirectional switch of the H-bridge includes the conducting transistor or diode.

The above introduced switching functions allow a unique general modeling approach to investigate both unfaulty and open-circuit faulty state of the considered power converter module. For this reason, let's suppose that the controllable upper device T_1 go to a drive failure condition. In this situation $Swf_{T1}=0$, and a positive current (from point *A* to *B*) cannot be conducted by the device. On the other hand, if the lower device T_2 is switched off a natural commutation appears and a negative current i_- may circulate in the upper diode D_1. Toward, if the transistor T_2 enters in the switch-on state the diode current turns again to zero. Results that the switching functions for the bidirectional switches can be written as follows [9, 10, 7]:

$$\begin{aligned} Swf_1{}' &= \overline{Swf_{T_2}} \odot i_- = Swf_{D_1} \\ Swf_2{}' &= Swf_{T_2} \odot i_- \end{aligned} \tag{9}$$

Very similar considerations can be also applied when the other three controllable devices of the H-bridge go to a drive failure condition. In order to express a general case it is possible to define a healthy device variable *h*, as it has been introduced in reference [7], with the following expression:

$$h_i = \begin{cases} 1\,, & if\ \ the\ electronic\ device\ h_i\ is\ healthy \\ 0\,, & otherwise,\ for\ j = 1 \div 4\,. \end{cases} \tag{10}$$

By introducing the h_i coefficient it is facilitated the generalization of equations (8), as is given below:

$$\begin{aligned} Swf_1 &= [h_1 \cdot Swf_{T_1} \odot i_+] \oplus [h_2 \cdot \overline{Swf_{T_2}} \odot i_-] \\ Swf_2 &= [h_2 \cdot Swf_{T_2} \odot i_-] \oplus [h_1 \cdot \overline{Swf_{T_1}} \odot i_+] \\ Swf_3 &= [h_3 \cdot Swf_{T_3} \odot i_+] \oplus [h_4 \cdot \overline{Swf_{T_4}} \odot i_-] \\ Swf_4 &= [h_4 \cdot Swf_{T_4} \odot i_-] \oplus \left[h_3 \cdot \overline{Swf_{T_3}} \odot i_+\right]. \end{aligned} \tag{11}$$

The above expressed equations define a generalized mathematical model of switching functions both for unfaulty and faulty state of the H-bridge from Fig. 1. It is important to mention here that the same principle is applied when both the transistor and free-wheeling diode enter into a failure condition. Additionally, in order to cover all the power electronic converter failure types, the case of a whole inverter leg loose also must be discussed. For this situation a very convenient solution can be obtained if a *healthy leg variable* it is introduced as follows [7, 8]:

$$h_{12} = h_1 \odot h_2\,, \tag{12}$$

if the devices T_1 and T_2go to a drive failure condition, respectively

$$h_{34} = h_3 \odot h_4\,, \tag{13}$$

if the transistors T_3 and T_4 enters into a failure condition and the whole leg is broken. It is possible to observe that this case does not introduce difference with respect to the previously considered, the *healthy leg variable* offering an easy and affordable modeling of the failure state. However, in such a situation usually the inverter hardware it is reconfigured by isolating the faulty leg and replaced with a healthy one. In this way the reconfiguration the power electronic converter enters into a fault-tolerant operation mode.

Considering the above discussed generalized switching model for unfaulty and faulty operation mode of the converter, the mathematical expressions (1) and (2) can be rewritten as the fault-tolerant system equations:

$$u(t) = \begin{cases} (Swf_1 \odot Swf_3) \cdot (+U_s)\ if\ i(t) \le i_{min} \\ (Swf_2 \odot Swf_4) \cdot (-U_s)\ if\ i(t) \ge i_{max} \end{cases} \tag{14}$$

$$i(t) = \begin{cases} \dfrac{(Swf_1 \odot Swf_3) \cdot U_s - E}{R} \cdot \left(1 - e^{-\frac{t}{\tau}}\right) + i_{min} \cdot e^{-\frac{t}{\tau}}, \\ 0 < t < T_c \\ -\dfrac{(Swf_2 \odot Swf_4) \cdot U_s + E}{R} \cdot \left(1 - e^{-\frac{t-T_c}{\tau}}\right) + \\ + i_{max} \cdot e^{-\frac{t-T_c}{\tau}}, \quad T_c < t < T \end{cases} \tag{15}$$

Summarizing the generalized mathematical model introduced in this paragraph, it is possible to conclude that it is well suitable to merge the two operation modes of the converter (unfaulty and faulty state) into a single simulation model. At the same time, allows considering several faulty simulation cases, such as: drive failure on a single device with current circulation on the free-wheeling diode corresponding to the interrupted device, simulation of faults on both the controllable device and its free-wheeling diode, or simulation of a whole inverter leg lose.

IV. THE MATHEMATICAL MODEL VALIDATION VIA COMPUTER-AIDED SIMULATIONS

The fault-tolerant power electronic converter model developed and presented in the previous paragraph has been validated via careful simulations in Matlab/Simulink software environment. In the first step of this research effort let's consider the Simulink block diagram for the unfaulty open-loop operation mode of a hybrid stepper motor driven by sinusoidal waveforms, as is shown next in Fig. 3. The motor phases are supplied via a PWM bang-bang inverter embedding two H-bridge configuration power electronic units with free-wheeling diodes. During the entire simulations will be followed the main state variables of the two-phase bipolar stepper motor: the phase currents i_1 and i_2 the phase supply voltagesU_1 and U_2, the electromagnetic torque T_e, the rotor velocity *w*, and the rotor angular position *Theta*.

In Fig. 4 it is presented the first simulation result set in unfaulty converter operation mode. There the supply voltages switching, the modulated phase currents, the electromagnetic torque waveform, or the rotor angular speed with low oscillations can be observed. The rotor angular position also increases smoothly.

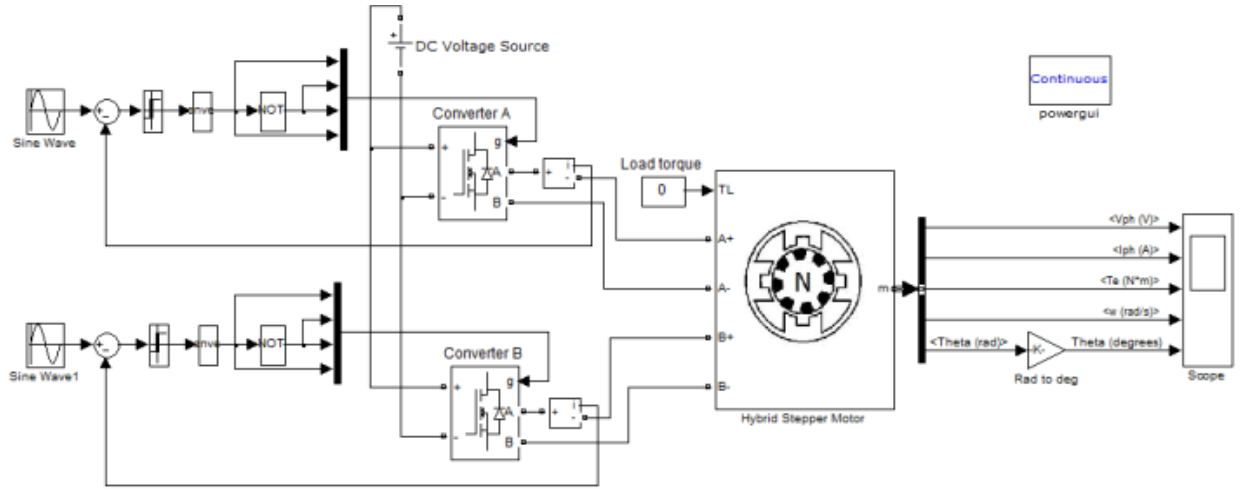

Figure 3. The Simulink block diagram of the hybrid stepper motor control system

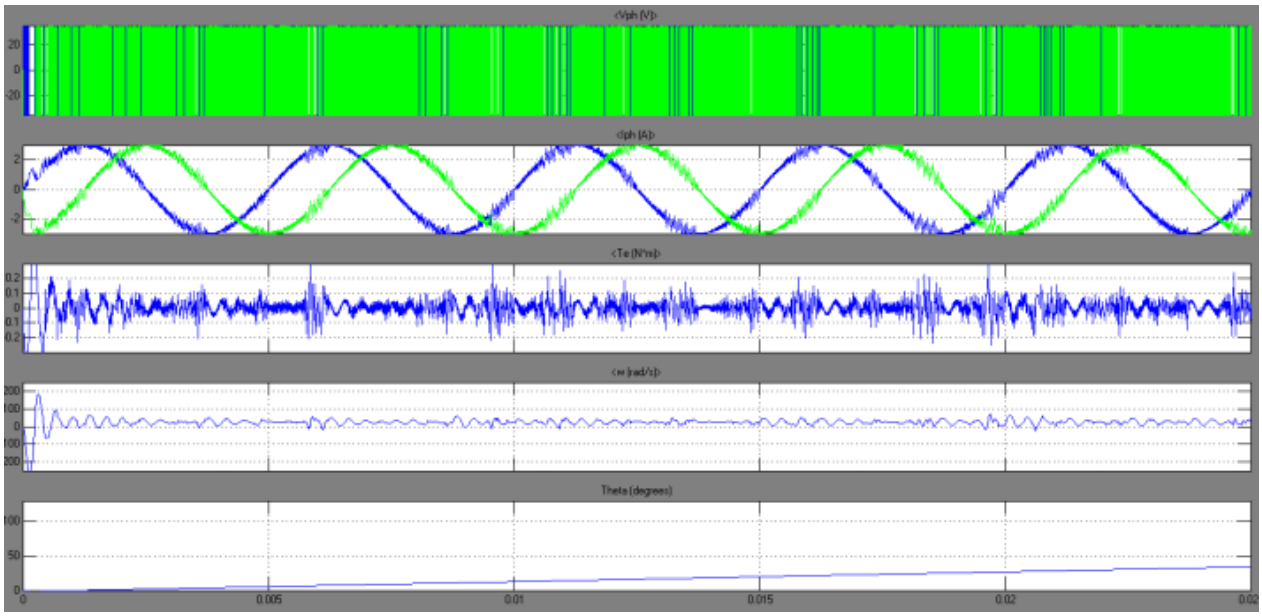

Figure 4. Waveforms of the hybrid stepper motor state variables in unfaulty operation mode

Fig. 5 shows the Simulink block diagram of the hybrid stepper motor control system when the controllable upper device $Mosfet_1$ go to a drive failure condition. In this situation it is considered that both the MOSFET transistor T_1 and its free-wheeling diode D_1 connected in parallel enters in a faulty state by producing an open circuit fault in the first leg of the H-bridge A. The waveforms set corresponding to this faulty situation is presented next in Fig. 6. It is no difficult to observe that during the positive period of the sinusoidal waveform there is no current flow in phase A, respectively the electromagnetic torque and rotor velocity ripples are high, the motor angular position oscillations are significant. This means that the devices failure introduces unwanted noises in these waveforms, and the motor running conditions has been deteriorated in a great manner. The above presented situation is getting worse if a power converter leg fault is simulated. Let's suppose now that both the controllable devices $Mosfet_1$ and $Mosfet_2$(T_2 and its free-wheeling diode D_2) simultaneously enter into a drive failure condition. In other words, emerges the situation of an electronic converter leg fault. The waveforms set corresponding to this specific situation is expressed in Fig. 7. It is self-evident that in this case just only one phase of the stepper motor is supplied and the waveform ripples becomes higher than in previous case. Obviously, in this situation the motor can't start away from its initial position, expressing only periodical angular position oscillations.

However, the presented Simulink program allows the convenient and user-friendly simulation of all the failure states expressed using the general mathematical model developed for current-source PWM inverters. In general terms expressed, it is not necessary to manage separate programs for the system operation in healthy (unfaulty) or faulty states, it is sufficient only to merge the two operation modes of the converter into a single coherent simulation model.

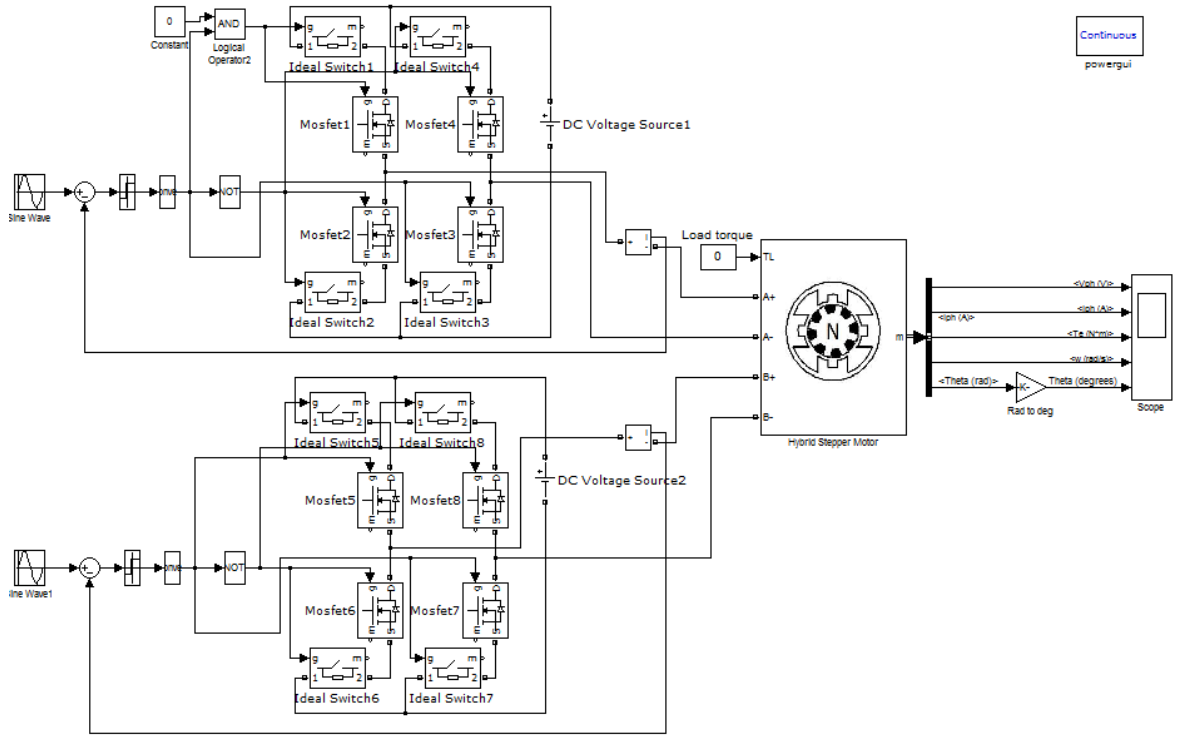

Figure 5. The Simulink block diagram of the hybrid stepper motor control system when both a switching device and diode fault occurs

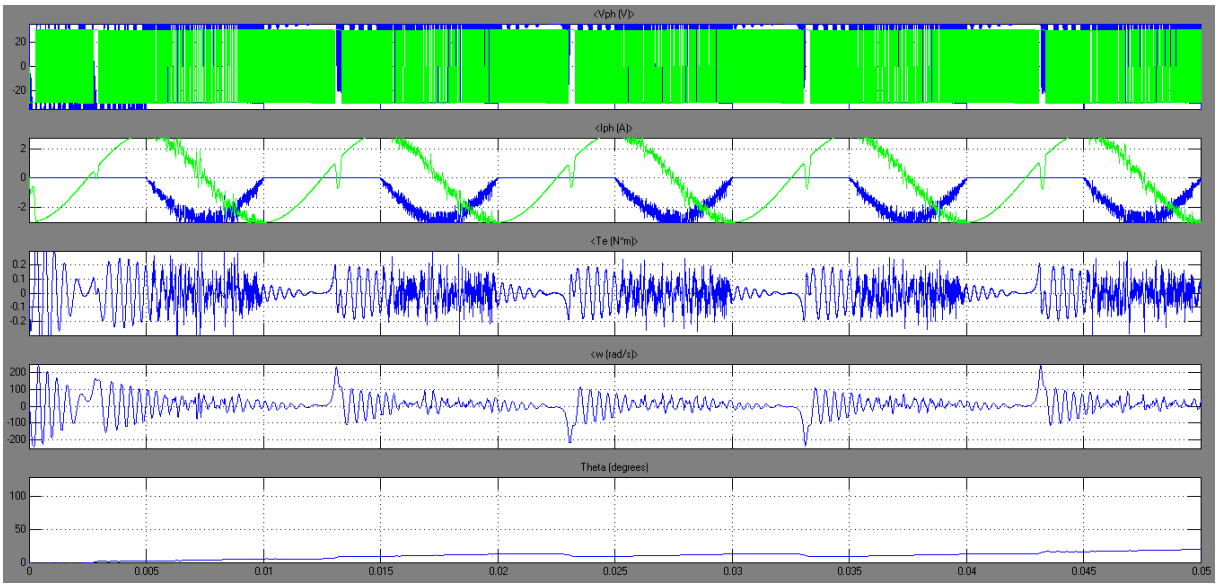

Figure 6. Waveforms of the hybrid stepper motor state variables in a converter faulty operation mode

Another important observation refers to the switching devices control strategy. There it must be outlined that in order to embed both healthy and faulty state operation of the power converter, the switching devices must be controlled in accordance with their individual switching functions expressed in the equation (11). From the programmer's side this means that the above mentioned equations should be implemented in simple Simulink blocks with outputs interfaced to drive the control pins of the power electronic devices.

The above presented simulation results implicitly raise the question of the fault-tolerant power converters design and development. This means the implementation of special converter topologies being able to cope with unwanted device failure states and to maintain its safety and proper operation mode even in presence of electronic components faults or when go to a drive failure condition. In such situations a good solution is the utilization of the reconfigurable architecture (or reconfigurable topology) power electronic structures. For example, in the specific case of the converter leg failure simulated in Fig. 7 is welcome the utilization of a redundant converter leg, ready to be interconnected once the $Mosfet_1$ and $Mosfet_2$ has entered in the failure state.

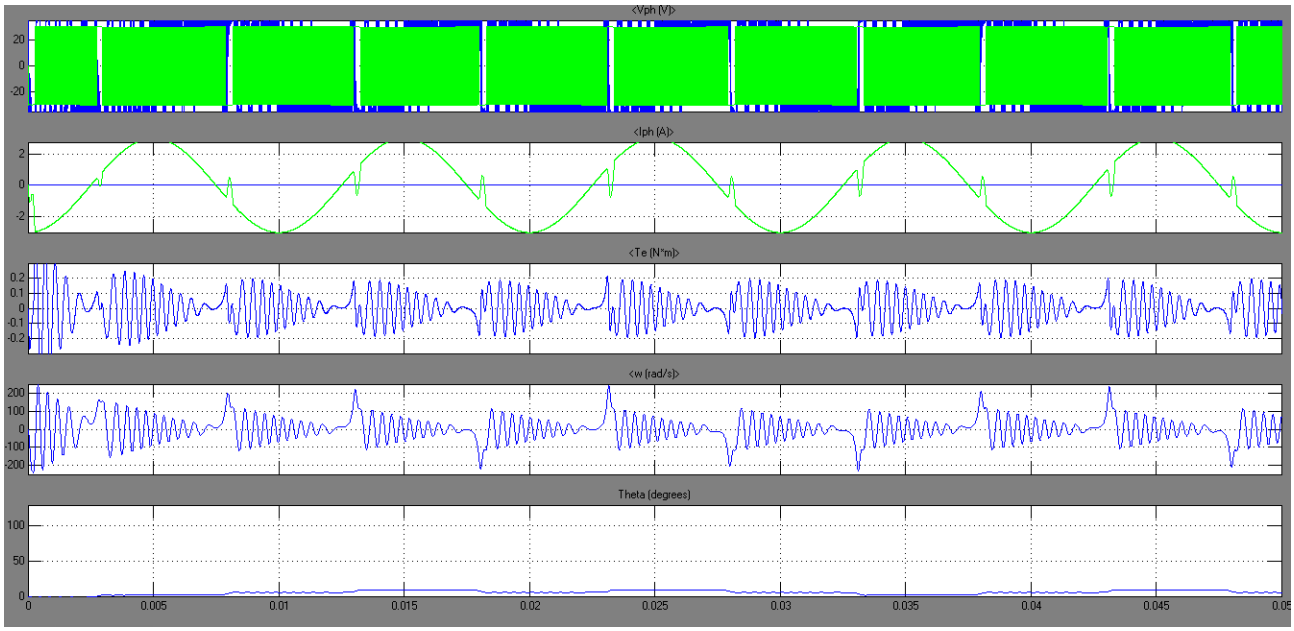

Figure 7. Waveforms of the hybrid stepper motor state variables in a converter leg-fault operation mode

V. CONCLUSIONS

The paper presents the mathematical model development for simulation of common faults in a current-source PWM inverter. This approach embeds into a single simulation module both the unfaulty or faulty states of this type of power electronic converter. The proposed model has been validated then via computer simulations. The introduced mathematical equations can serve as an adequate background for design and implementation of novel software toolkits suitable to simulate both healthy and faulty operation regime of power electronic systems. Future researches will be focused on development and experimentation of fault-tolerant power electronic converter topologies.

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